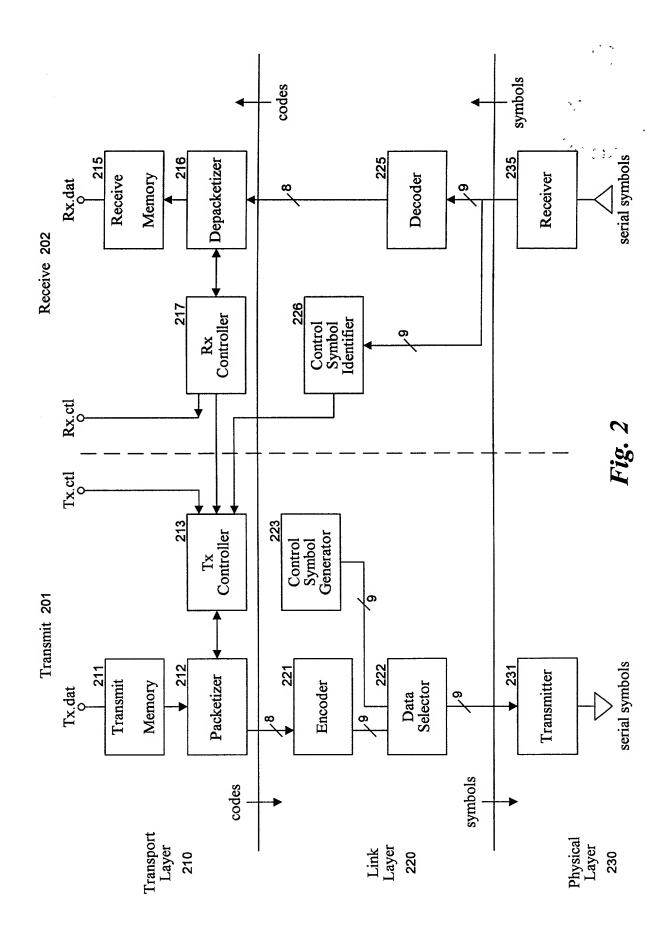
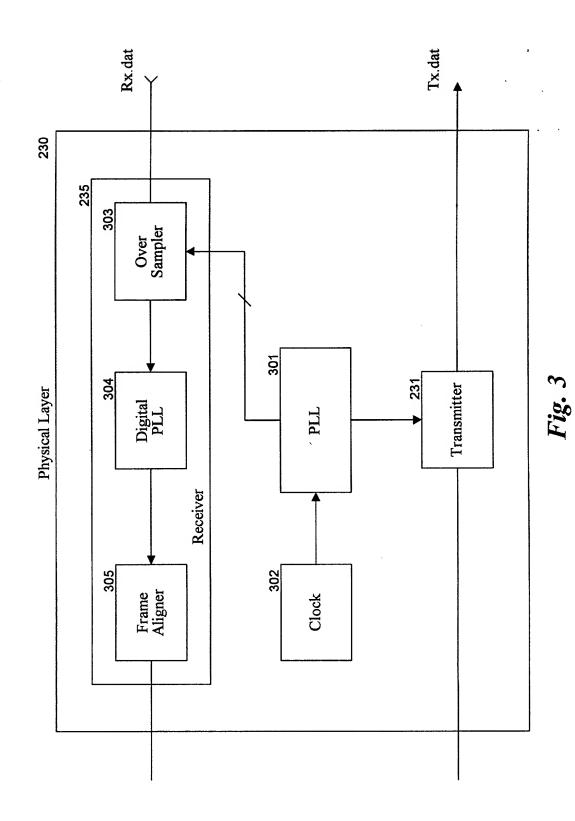


Fig. 1





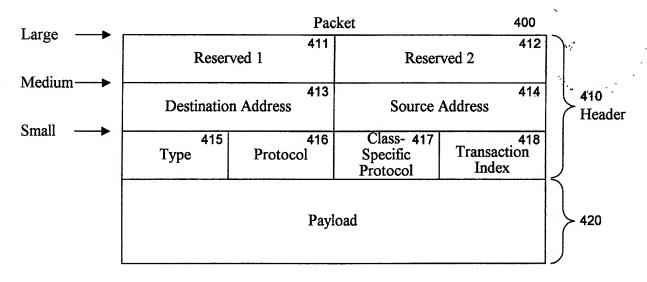


Fig. 4

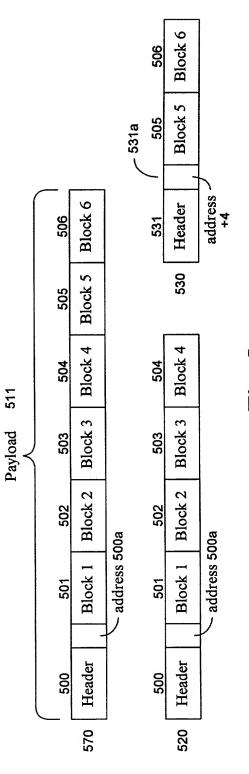


Fig. 5

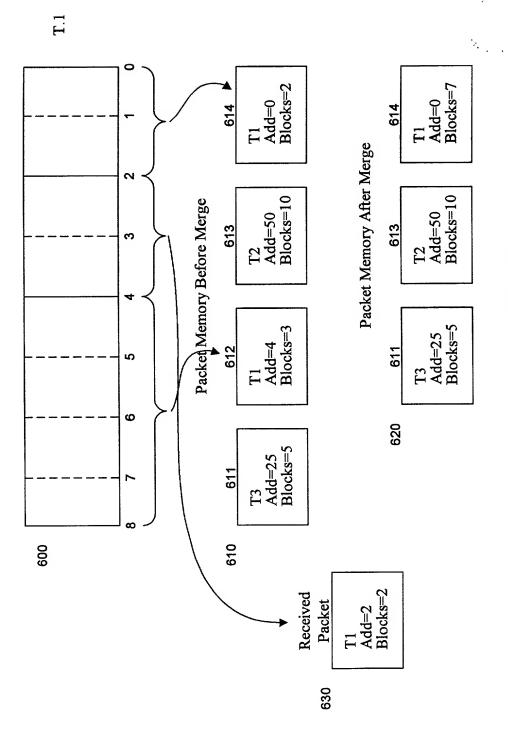
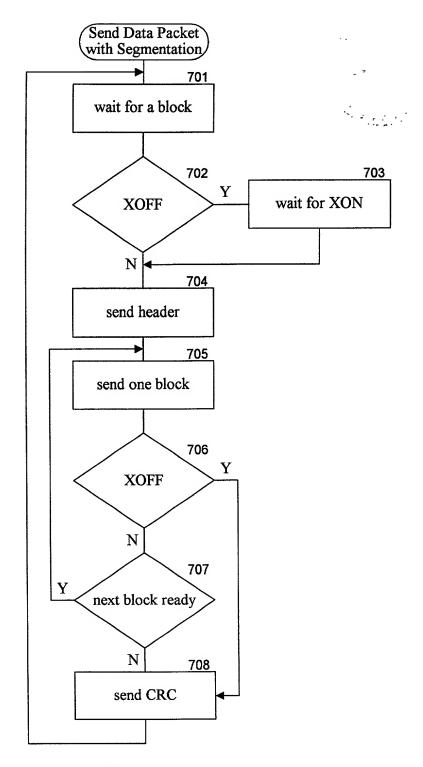
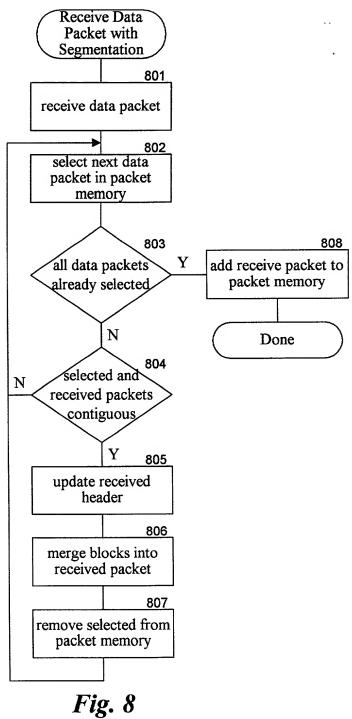
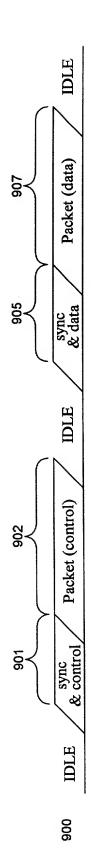


Fig. 6



*Fig.* 7





sync & packet type

Fig. 9A

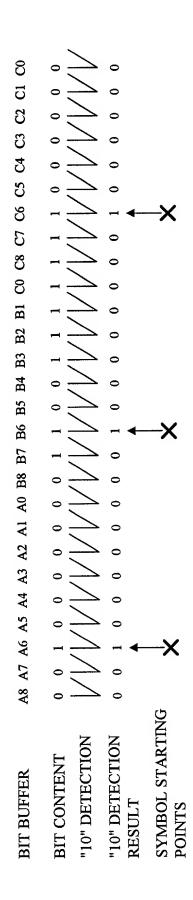


Fig. 9B

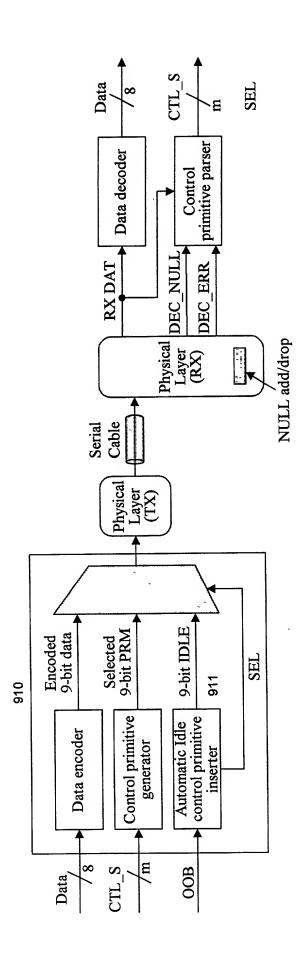
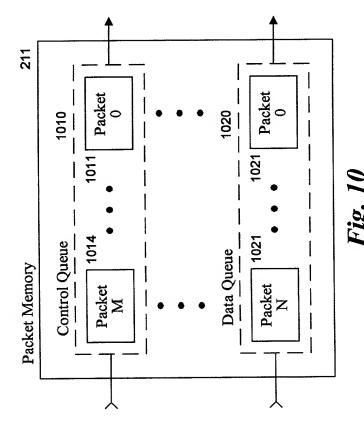


Fig. 9C



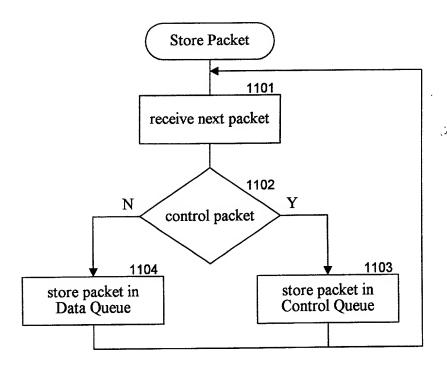


Fig. 11



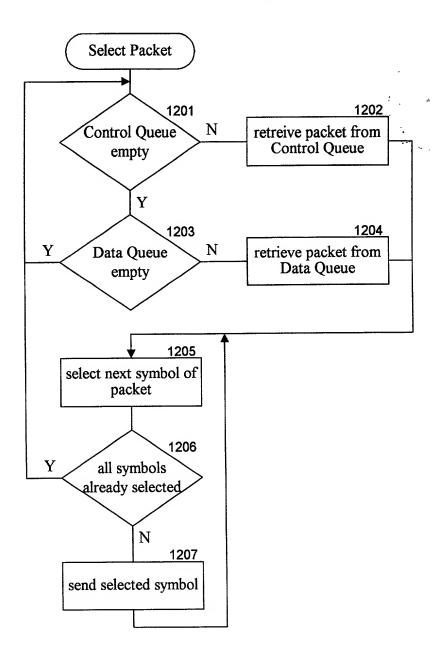


Fig. 12

•	IDLE	
1305	/ data /	packet (cont'd)
1304		commue
1303	control	packet
1302	,   	/ Preempt /
1301	data	packet /
	1	IDLE
	0	1300

Fig. 13

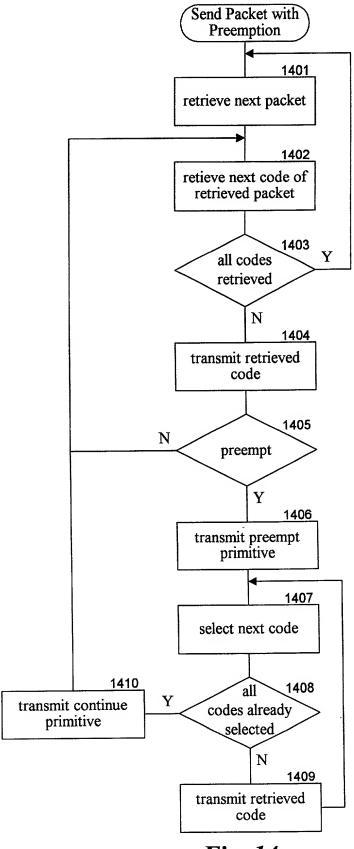


Fig. 14

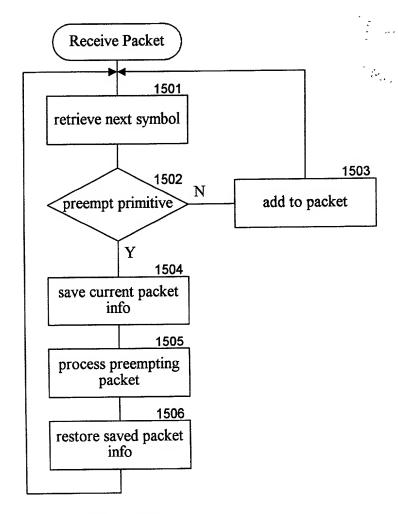


Fig. 15

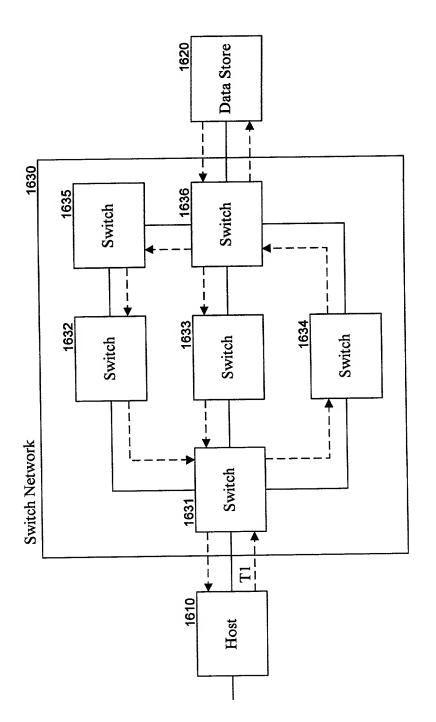


Fig. 16

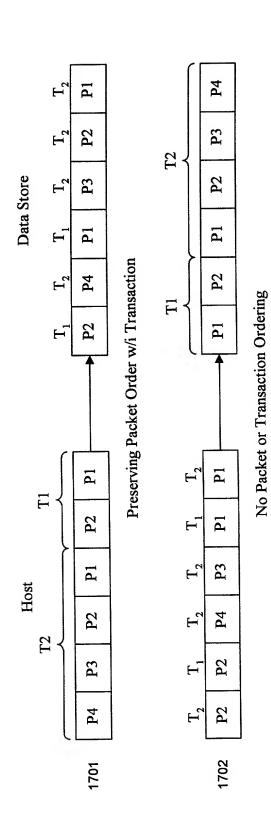


Fig. 17

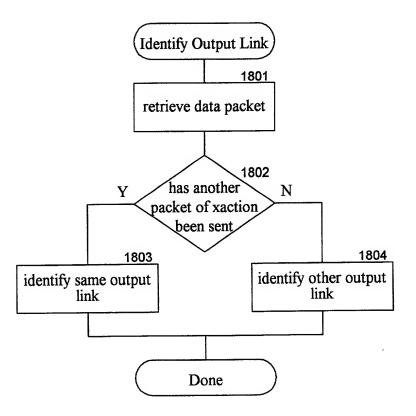


Fig. 18

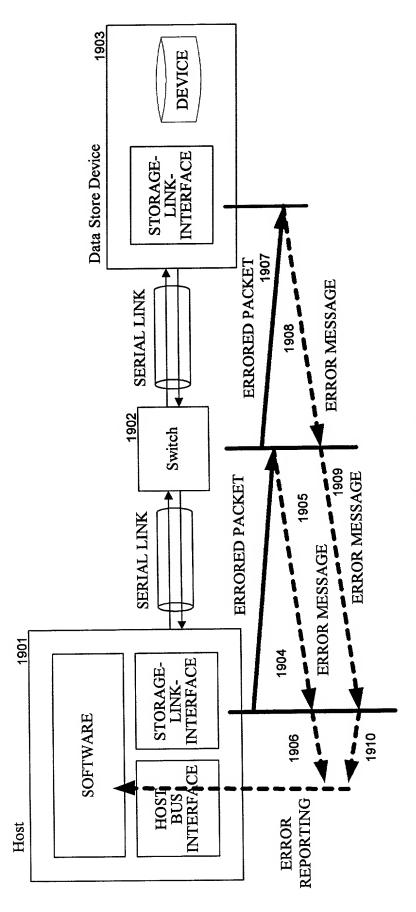
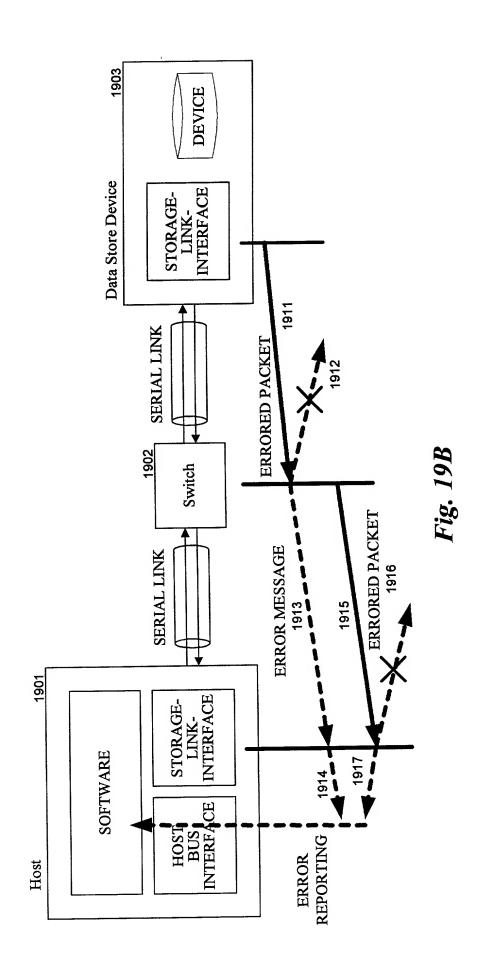


Fig. 19A

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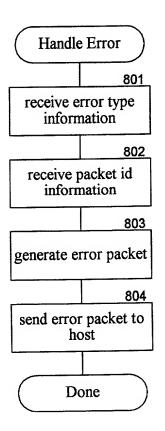


Fig. 19C

8b code		9 bit symbol
0000	0000	101010101
0000	0001	101010100
0000	0010	101010111
0101	0101	001010101
0111	0110	001110110
0111	0111	100100010
1111	1111	110101010

Fig. 20

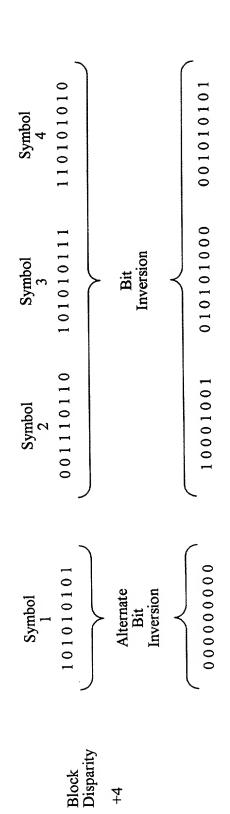
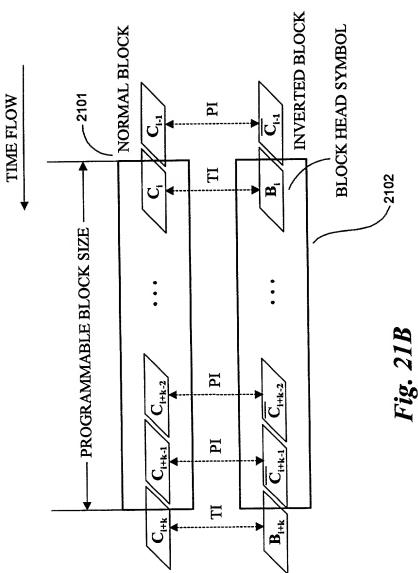


Fig. 21A



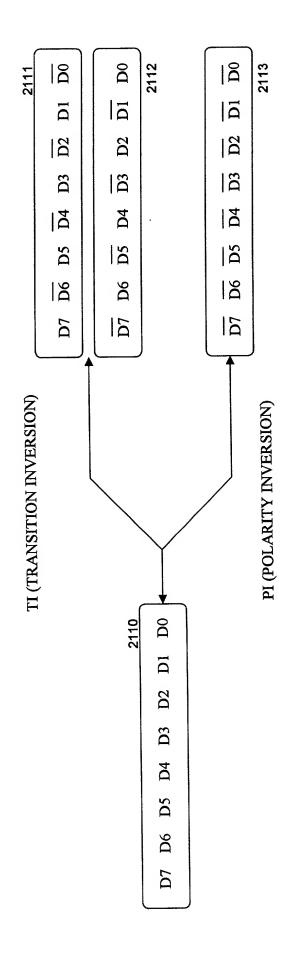


Fig. 21C

ngay or managagagagan

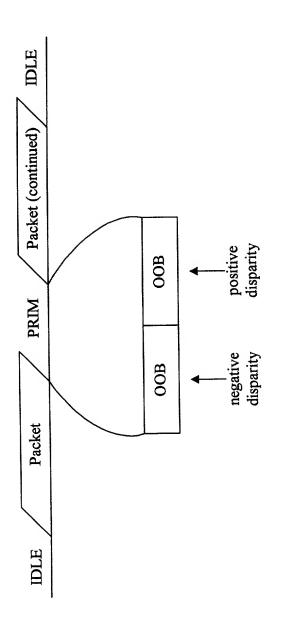


Fig. 22

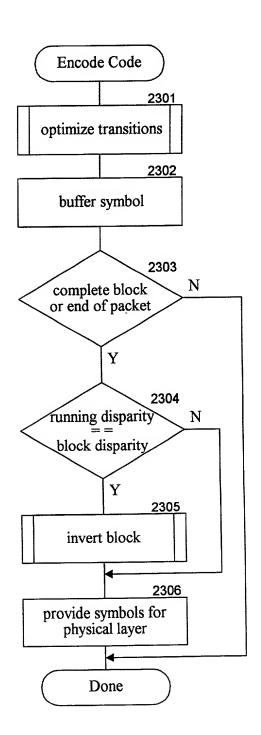


Fig. 23

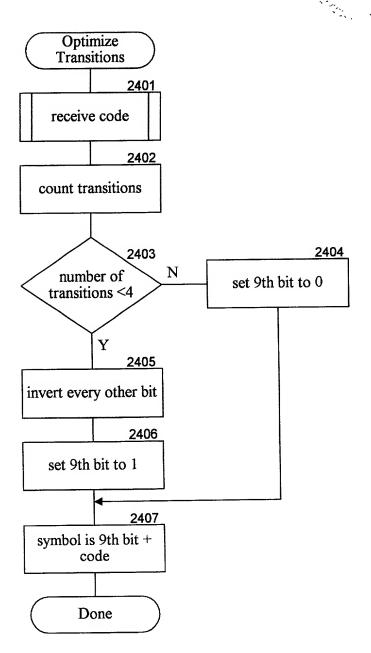


Fig. 24

MARIATER STATE

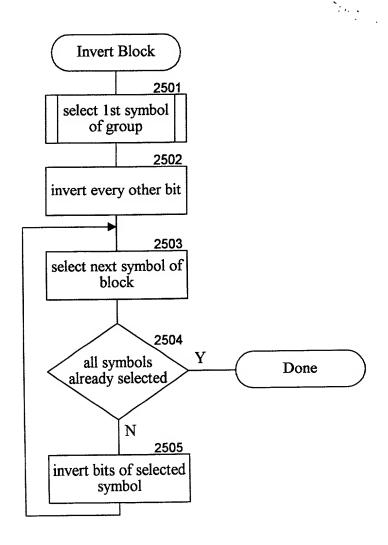
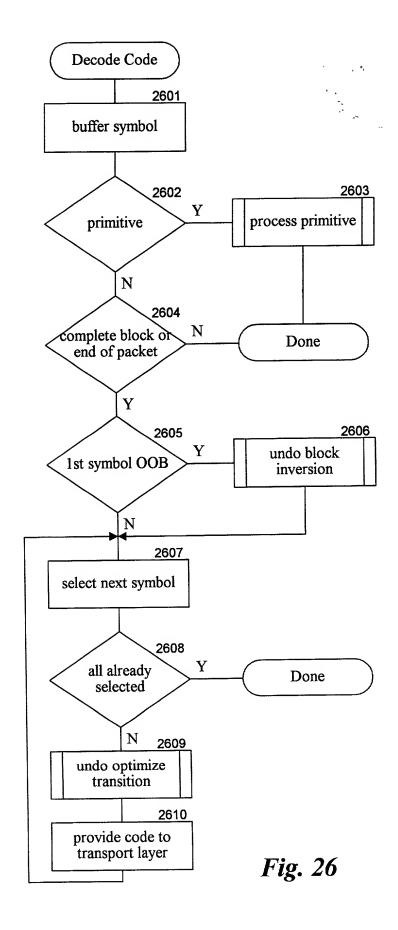


Fig. 25



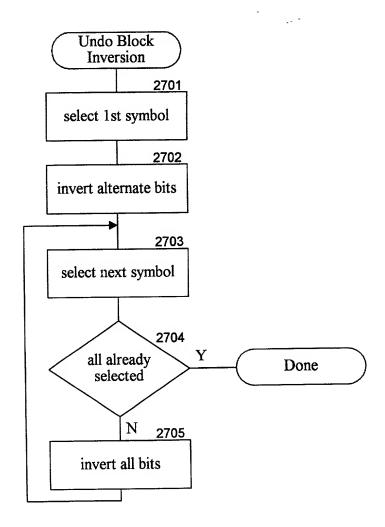


Fig. 27

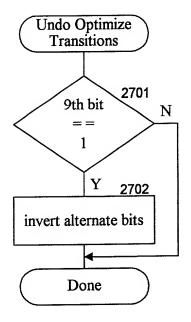


Fig. 28

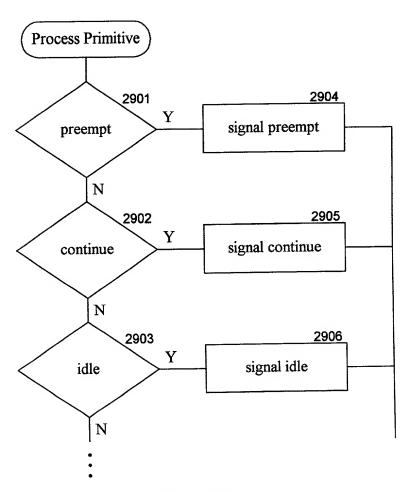
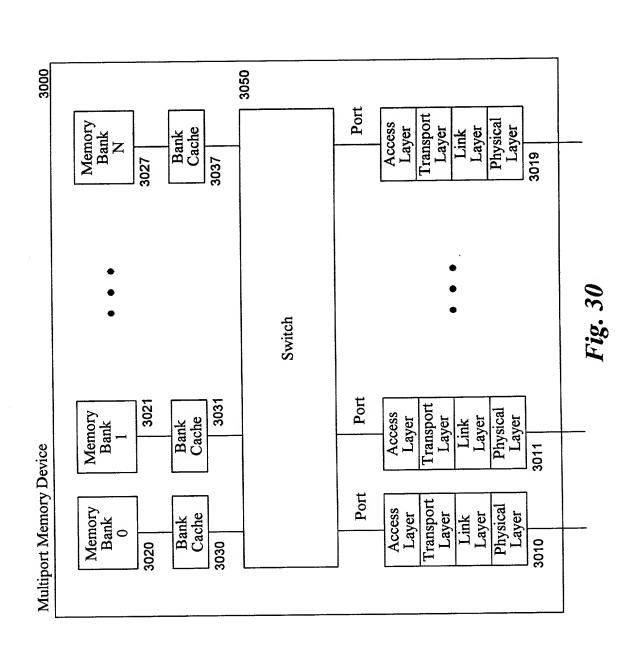


Fig. 29



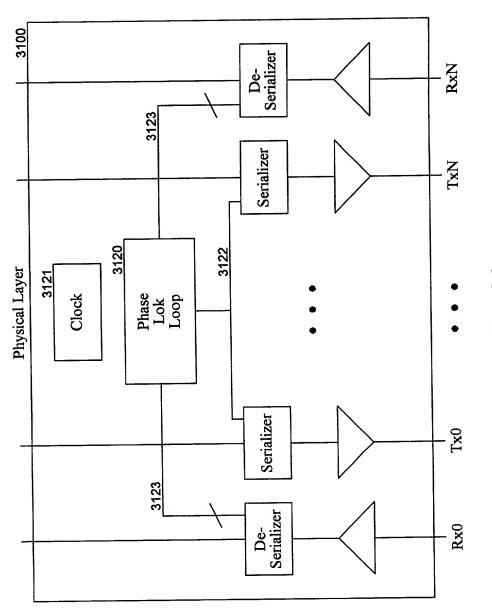


Fig. 3.

Output Queue 3202	Data	110			1011	
	Valid Port Data	3			3	• • •
	Valid	1	0	0	1	
	•					
3201	Data		101	1110		
Input Queue	R/W Address	1000	4000	1000	2000	
	R/W	8	W	W	R	• • •
	Port	3	4	3	3	

Fig. 32

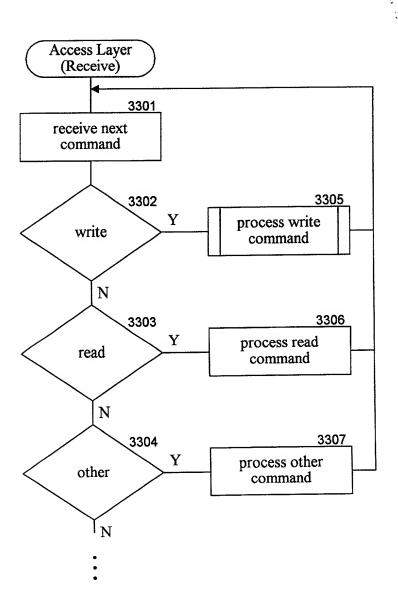


Fig. 33

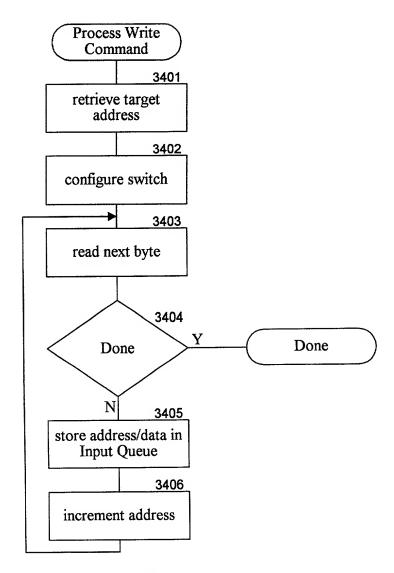


Fig. 34

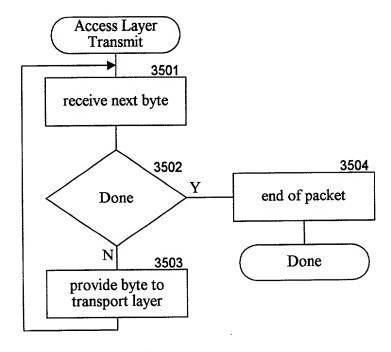
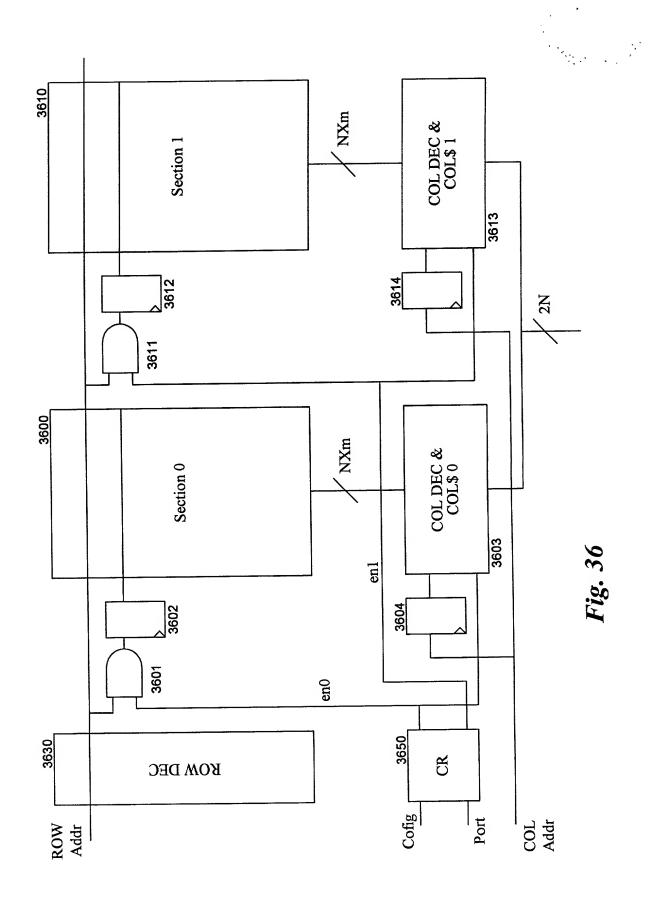


Fig. 35



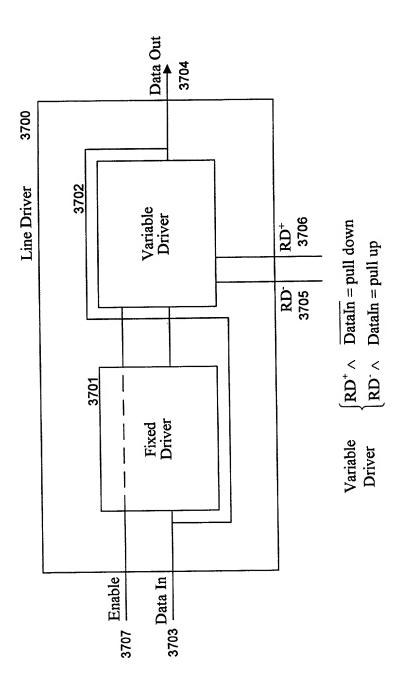


Fig. 37.4

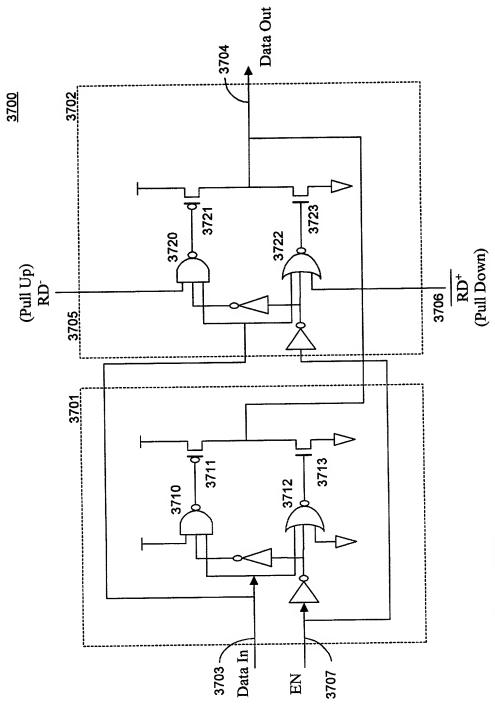


Fig. 37B

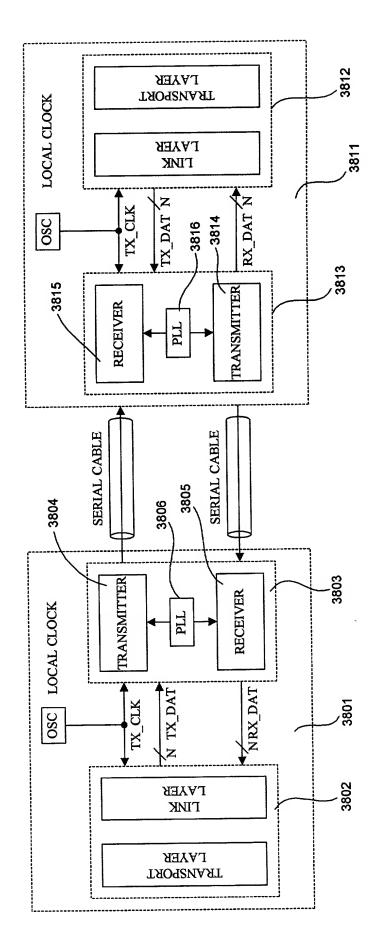


Fig. 38A

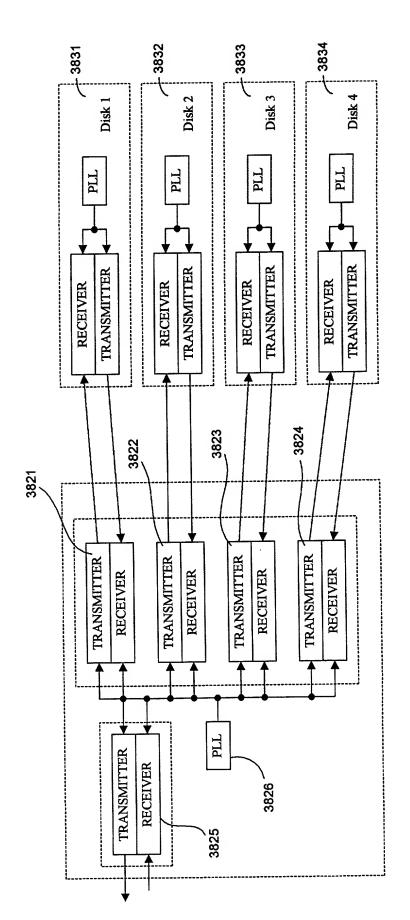
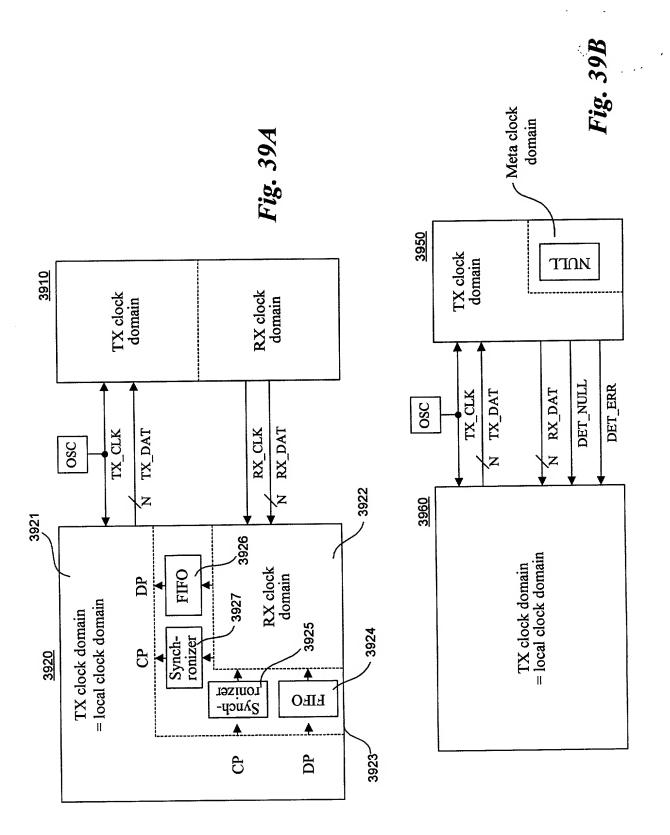
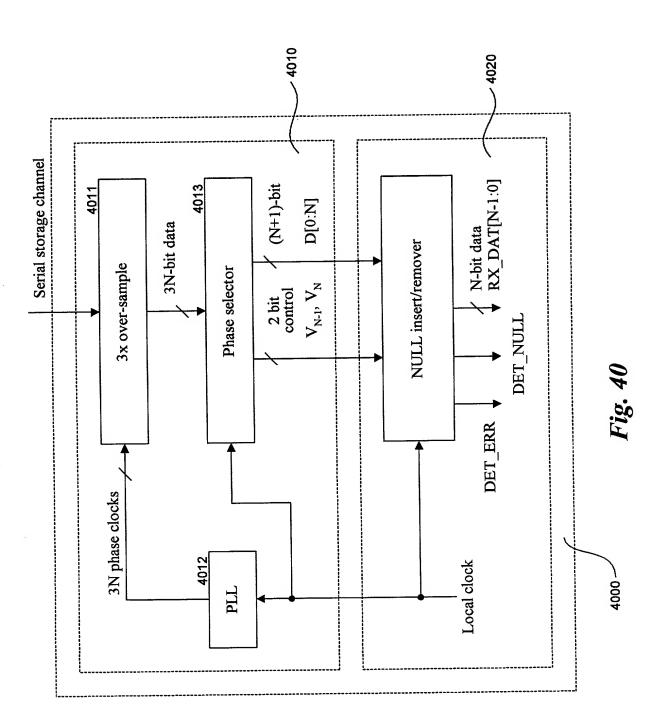


Fig. 38B





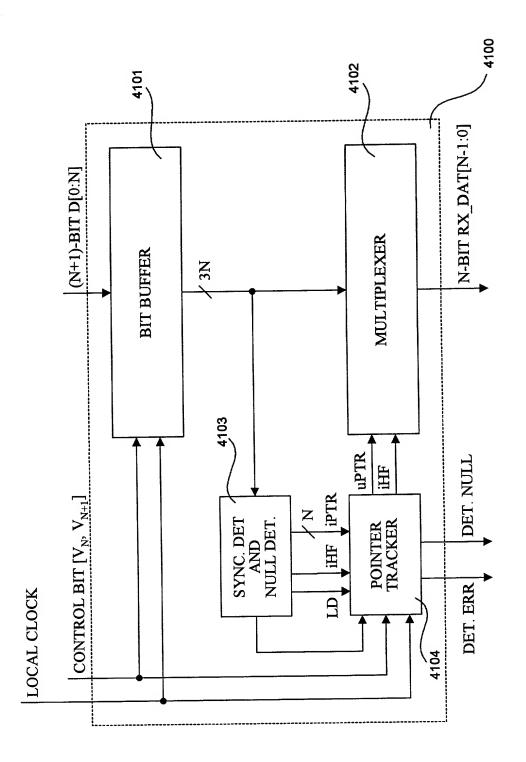
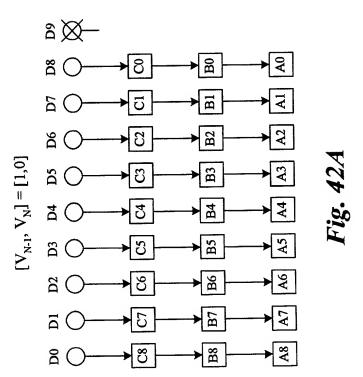


Fig. 4



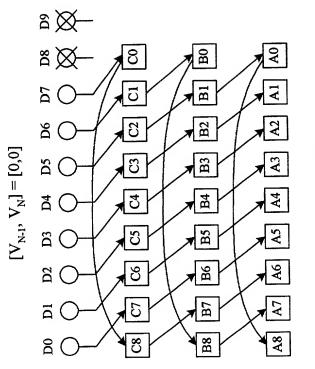


Fig. 42B

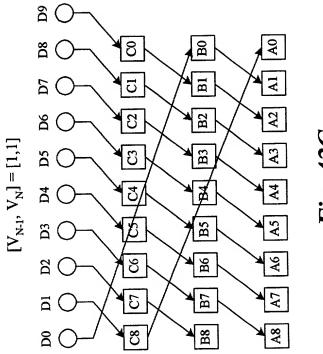


Fig. 42C

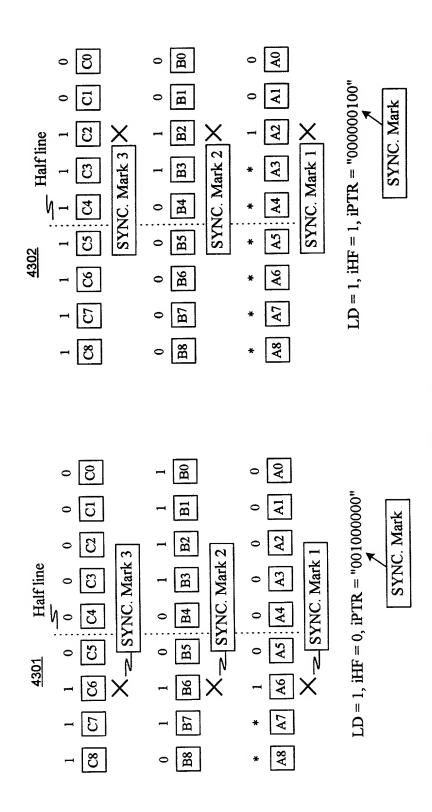
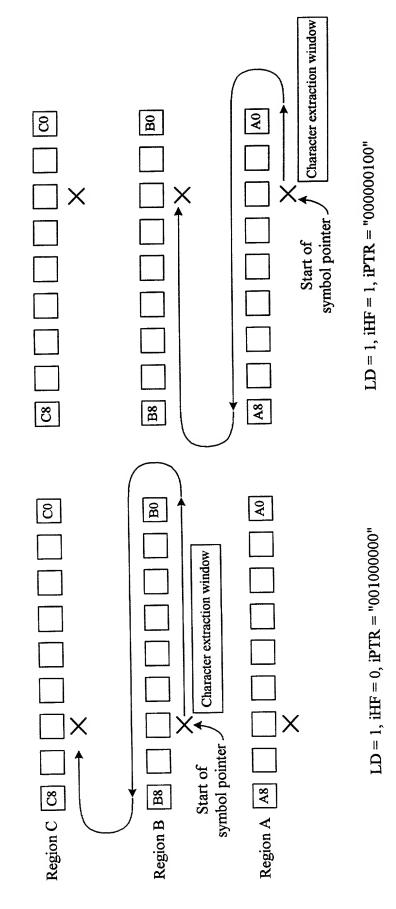
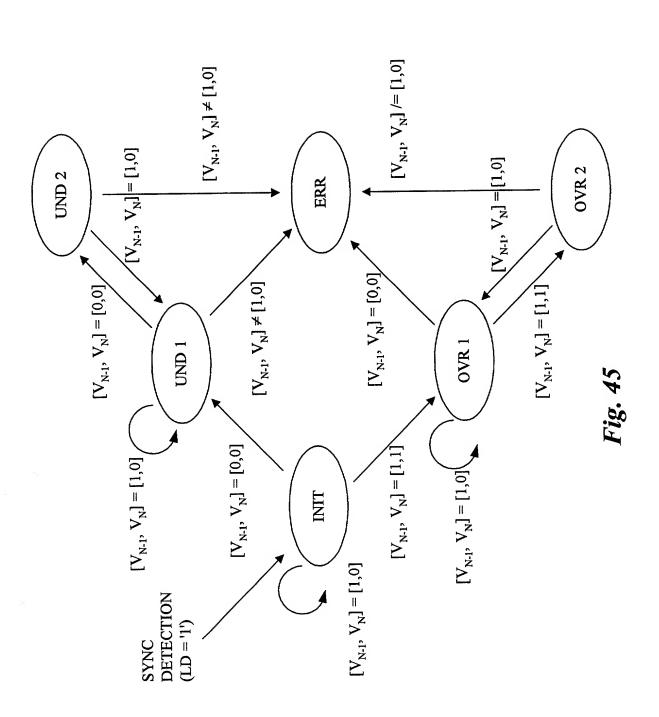


Fig. 43





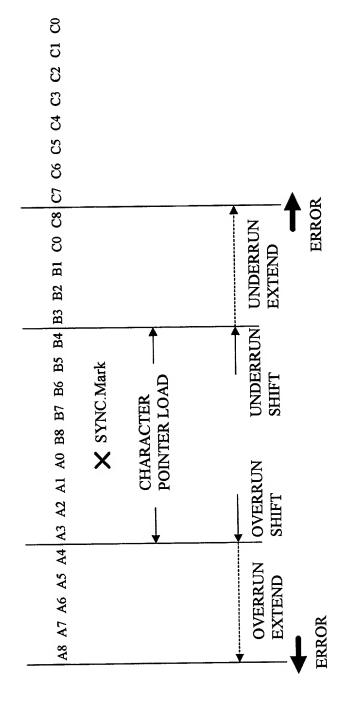


Fig. 46

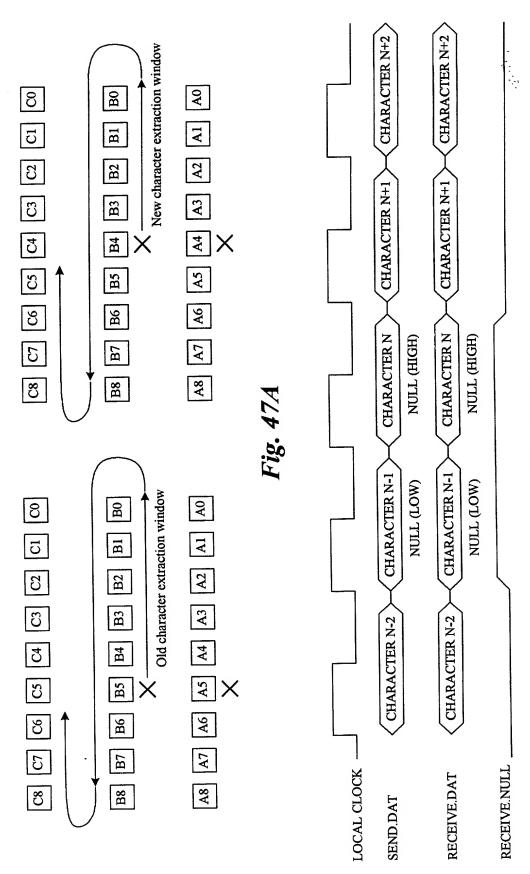


Fig. 47B

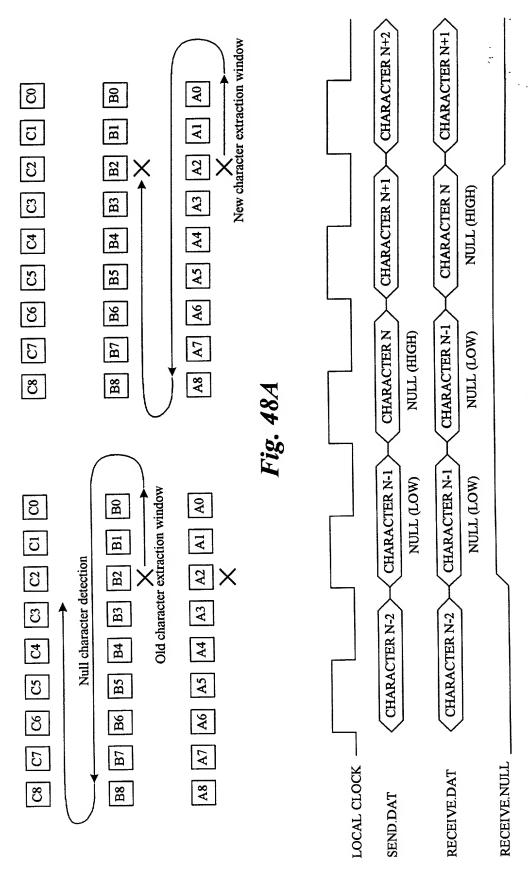


Fig. 48B

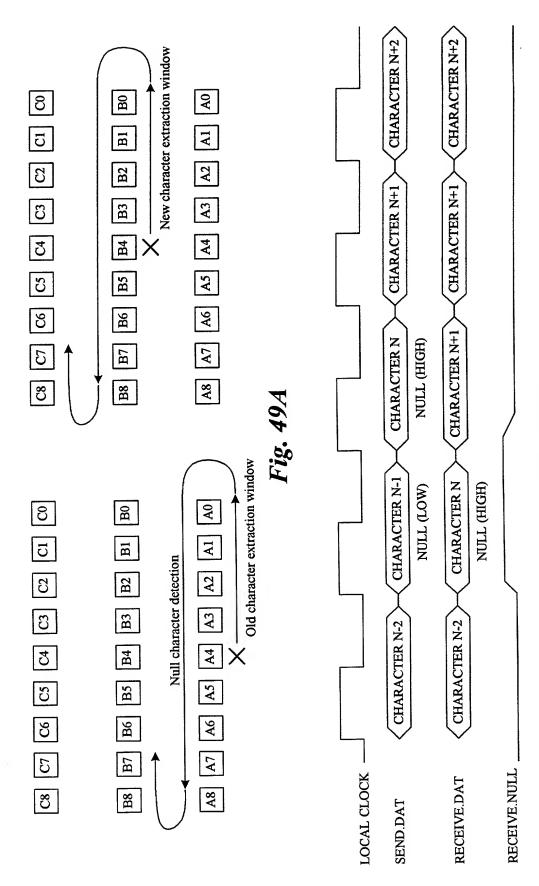


Fig. 49B